PCB DESIGN AND VERIFICATION FLOW (FOR DDR-IF)

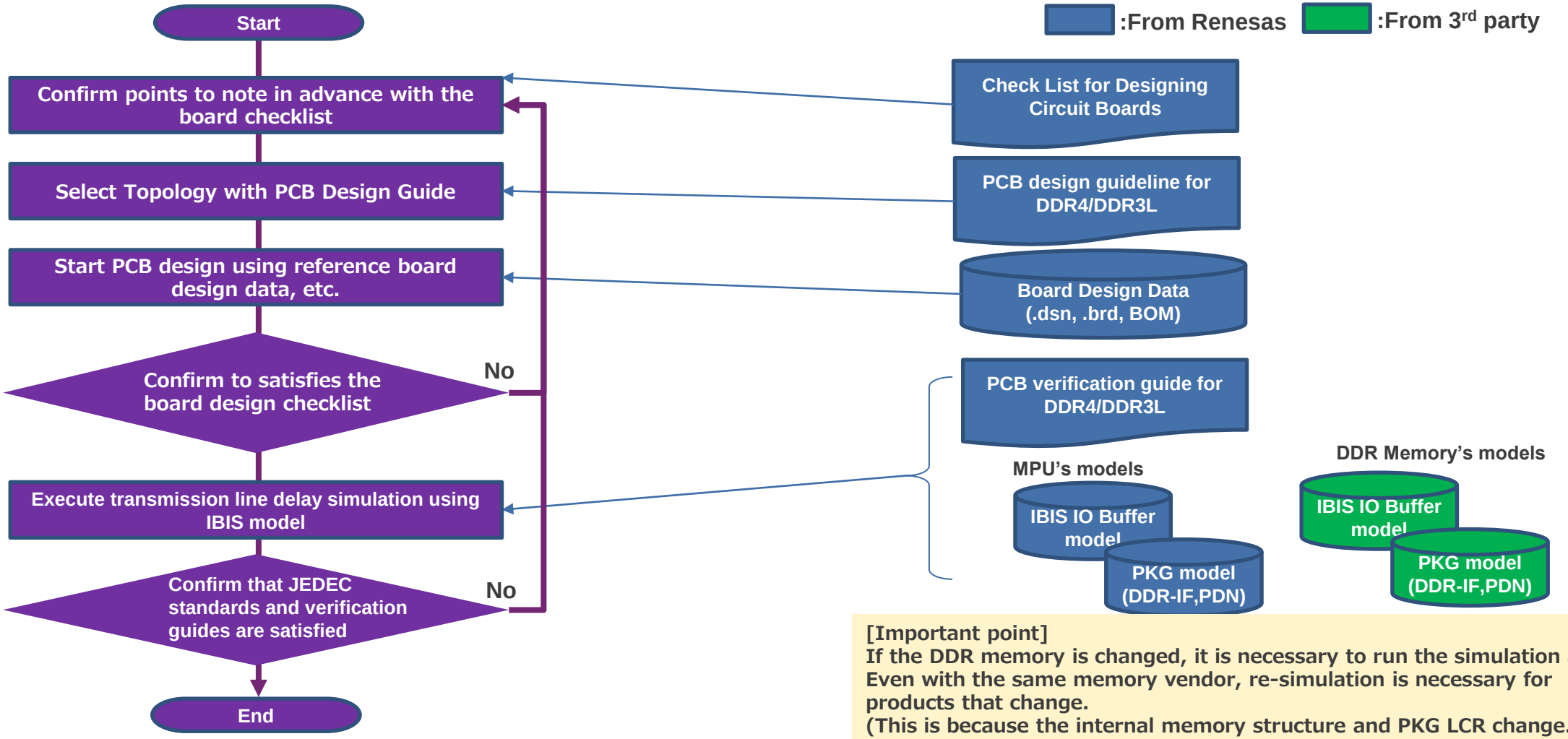
FLOW GUIDELINE (FOR CUSTOMER)

MARCH.2023 (REV1.0)

MPU BUSINESS DEVELOPMENT DEPARTMENT
ENTERPRISE INFRASTRUCTURE BUSINESS DIVISION
IOT & INFRASTRUCTURE BUSINESS UNIT
RENESAS ELECTRONICS COOPERATION

PCB DESIGN PHASE FOR DDR-IF PART

HOW TO USE HW DESIGN GUIDE AND MODEL

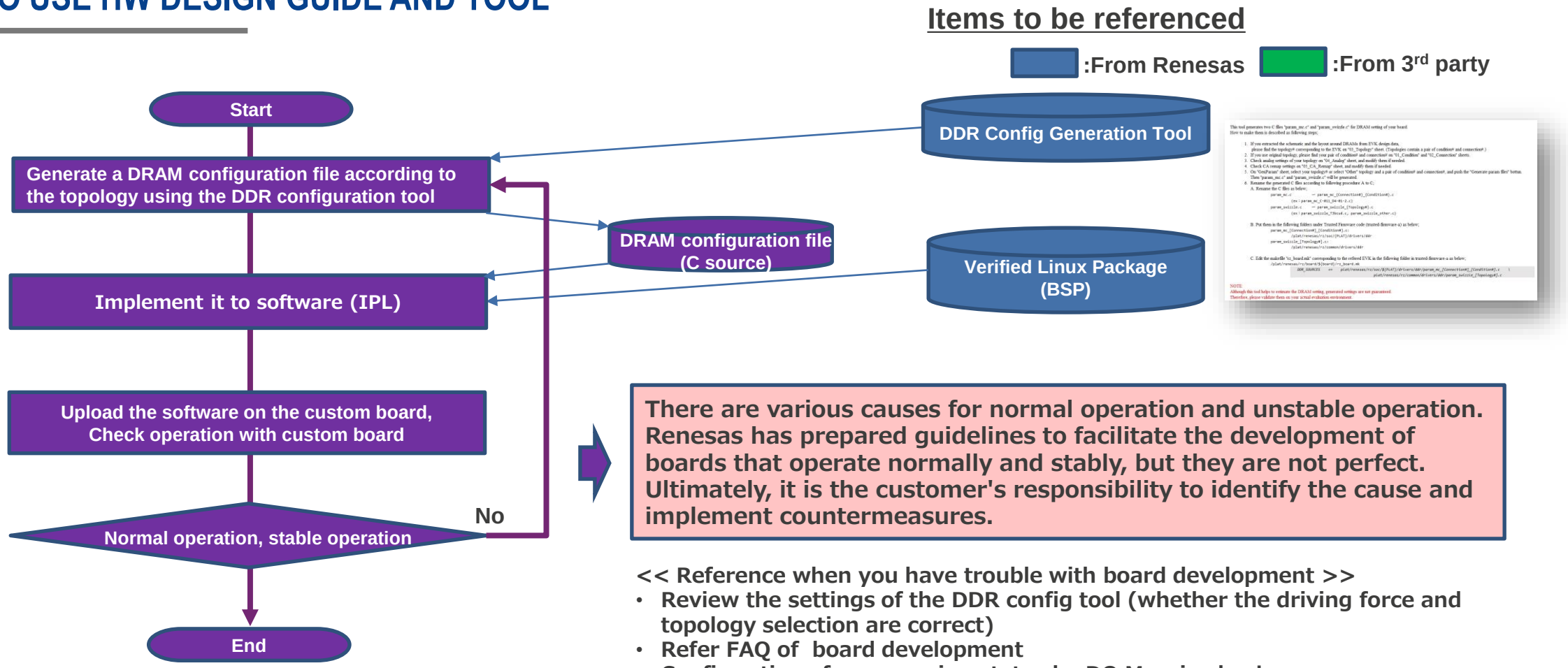


[Important point]
If the DDR memory is changed, it is necessary to run the simulation again.
Even with the same memory vendor, re-simulation is necessary for products that change.
(This is because the internal memory structure and PKG LCR change.)

Custom board trial production started ➡ Operation check after completing the board(See next page)

OPERATION CHECK OF CUSTOM BOARD FOR DDR-IF PART

HOW TO USE HW DESIGN GUIDE AND TOOL



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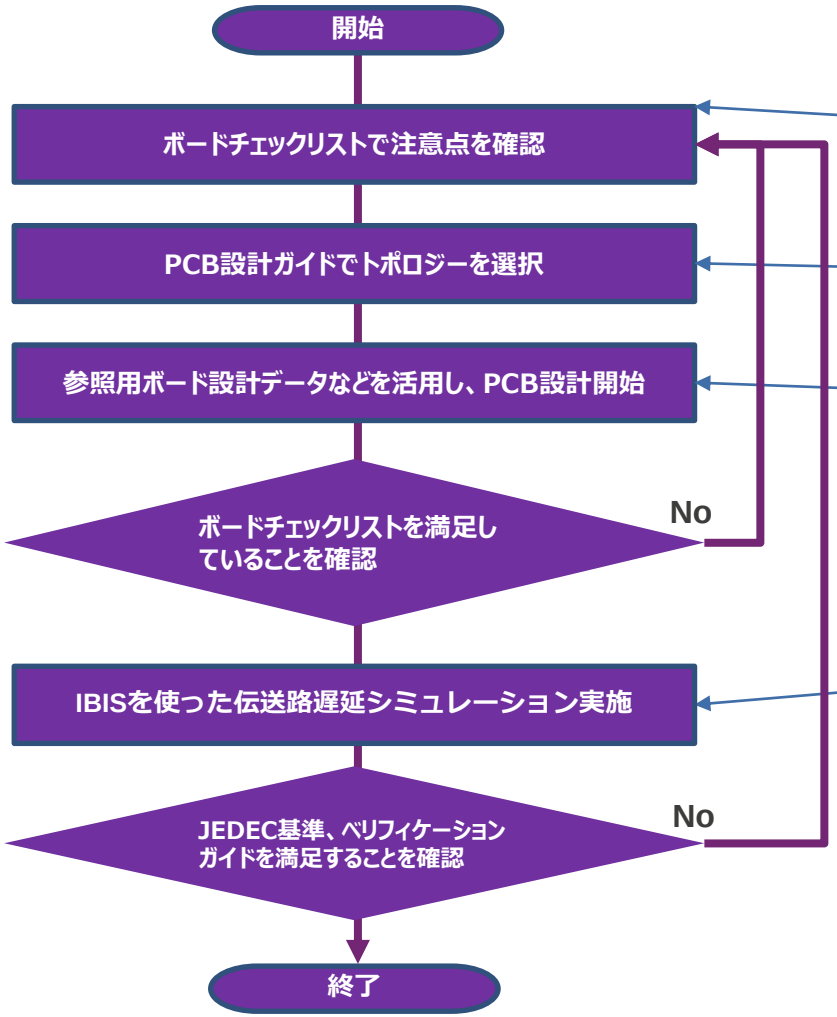


Items to be referenced

:From Renesas　:From 3rd party

- Check List for Designing Circuit Boards
- PCB design guideline for DDR4/DDR3L
- Board Design Data (.dsn, .brd, BOM)
- PCB verification guide for DDR4/DDR3L

MPU's models
- IBIS IO Buffer model
- PKG model (DDR-IF,PDN)

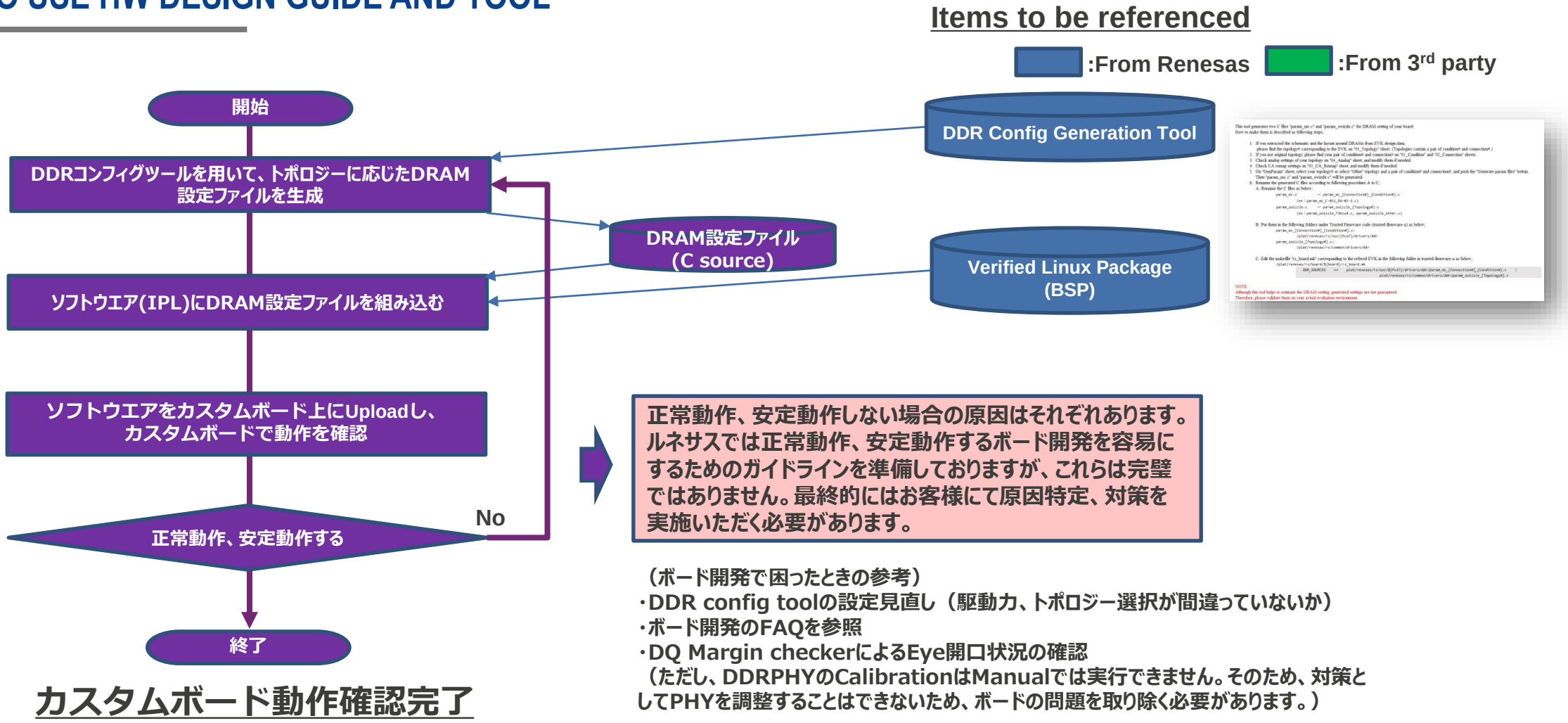
DDR Memory's models
- IBIS IO Buffer model
- PKG model (DDR-IF,PDN)

注意点
DDRメモリが変更された場合、再度、シミュレーションの実施が必要。
同じベンダでも製品が変わる再シミュレーションが必要です。
(メモリ内部の構造や、PKGのLCRが変わるため)

カスタムボード試作開始　➡　完成後、動作確認(次ページ参照)

OPERATION CHECK OF CUSTOM BOARD FOR DDR-IF PART

HOW TO USE HW DESIGN GUIDE AND TOOL



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